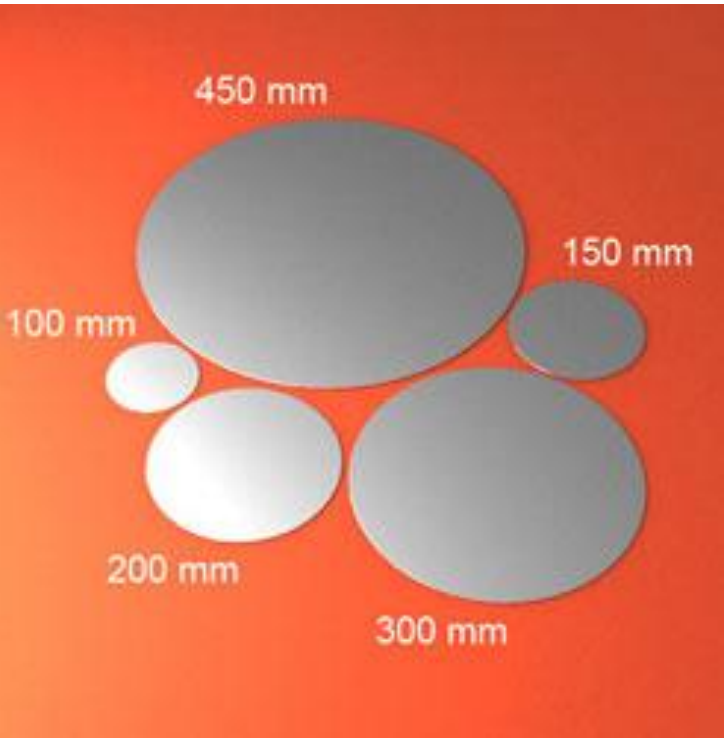
HOW TO CONTINUE COST SCALING



Hans Lebon

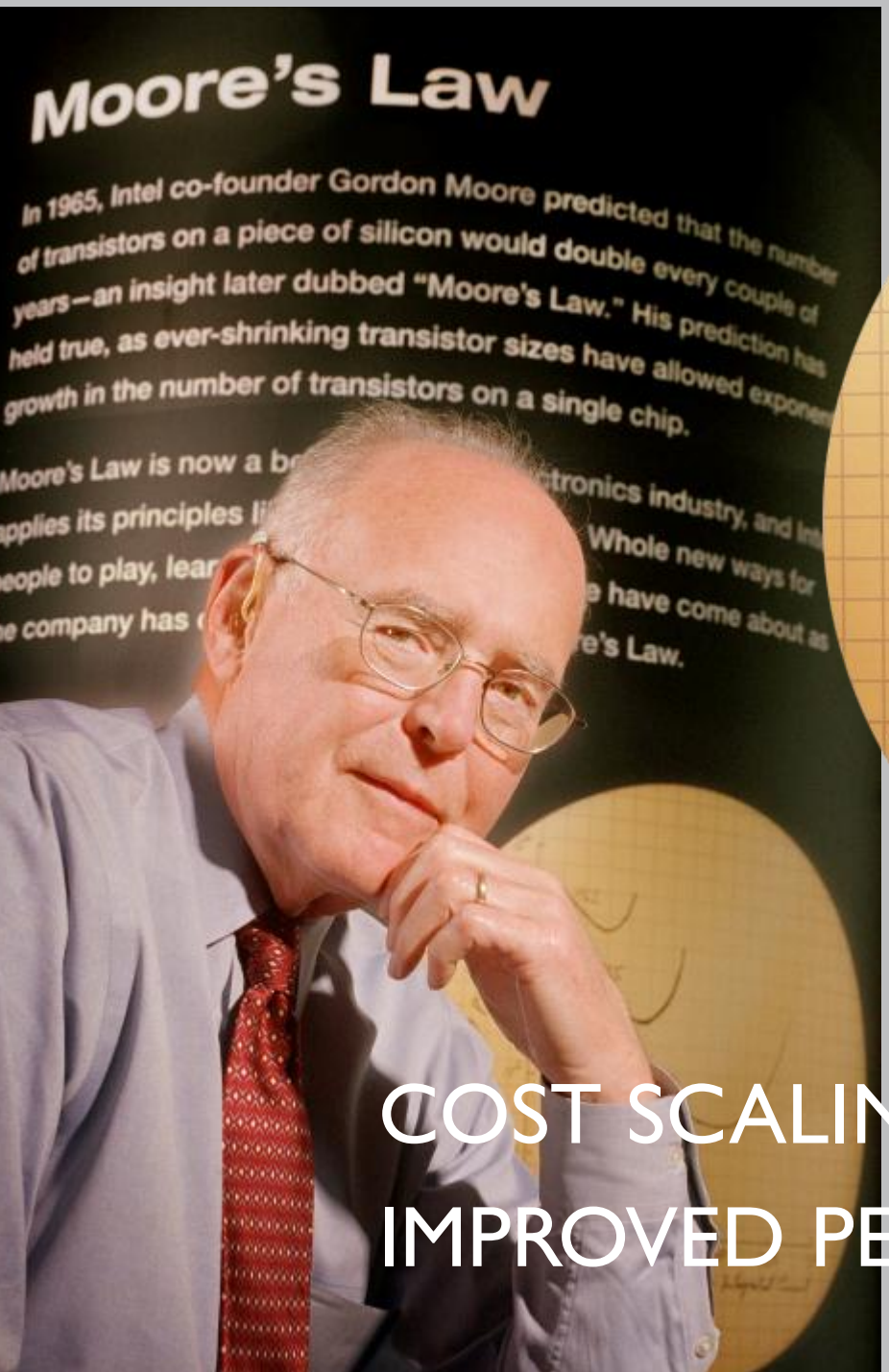
imec

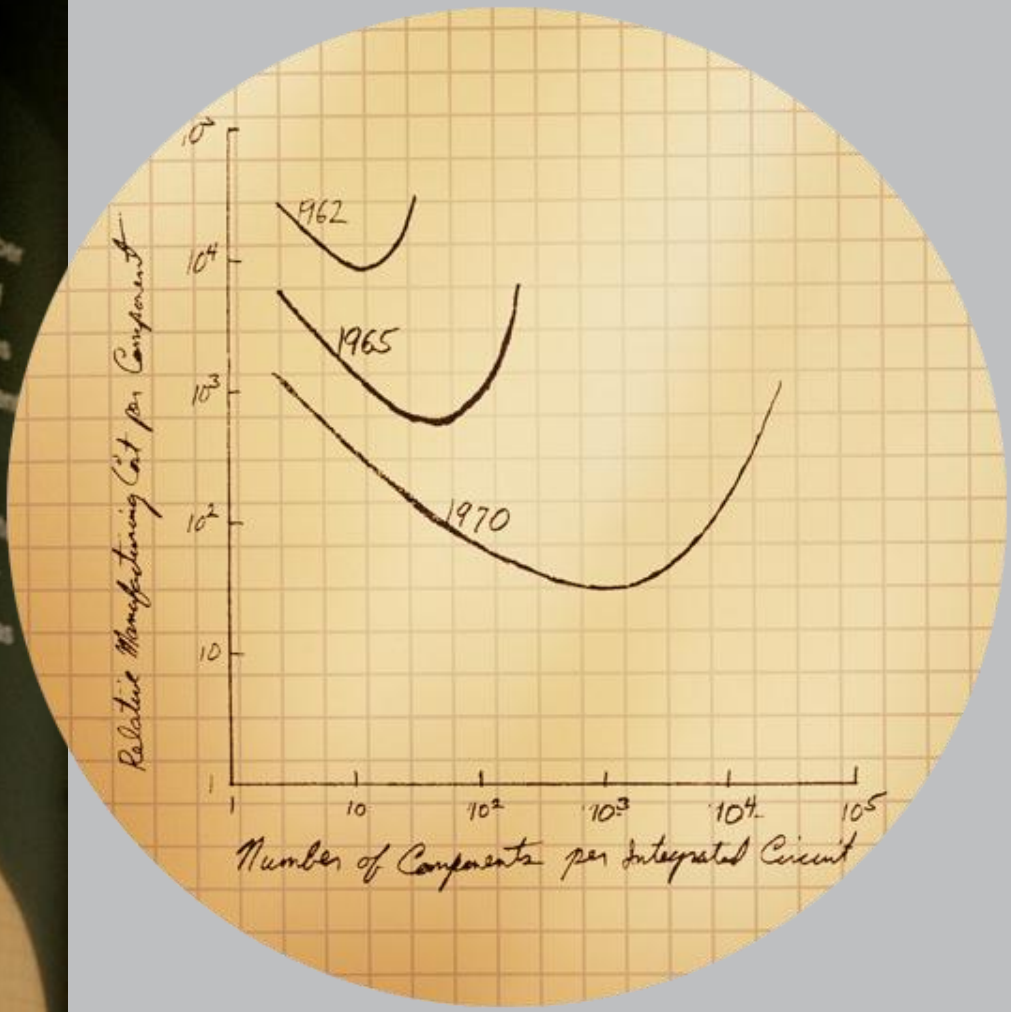
OUTLINE

Scaling & Scaling Challenges

Imec Technology Roadmap

Wafer size scaling : 450 mm



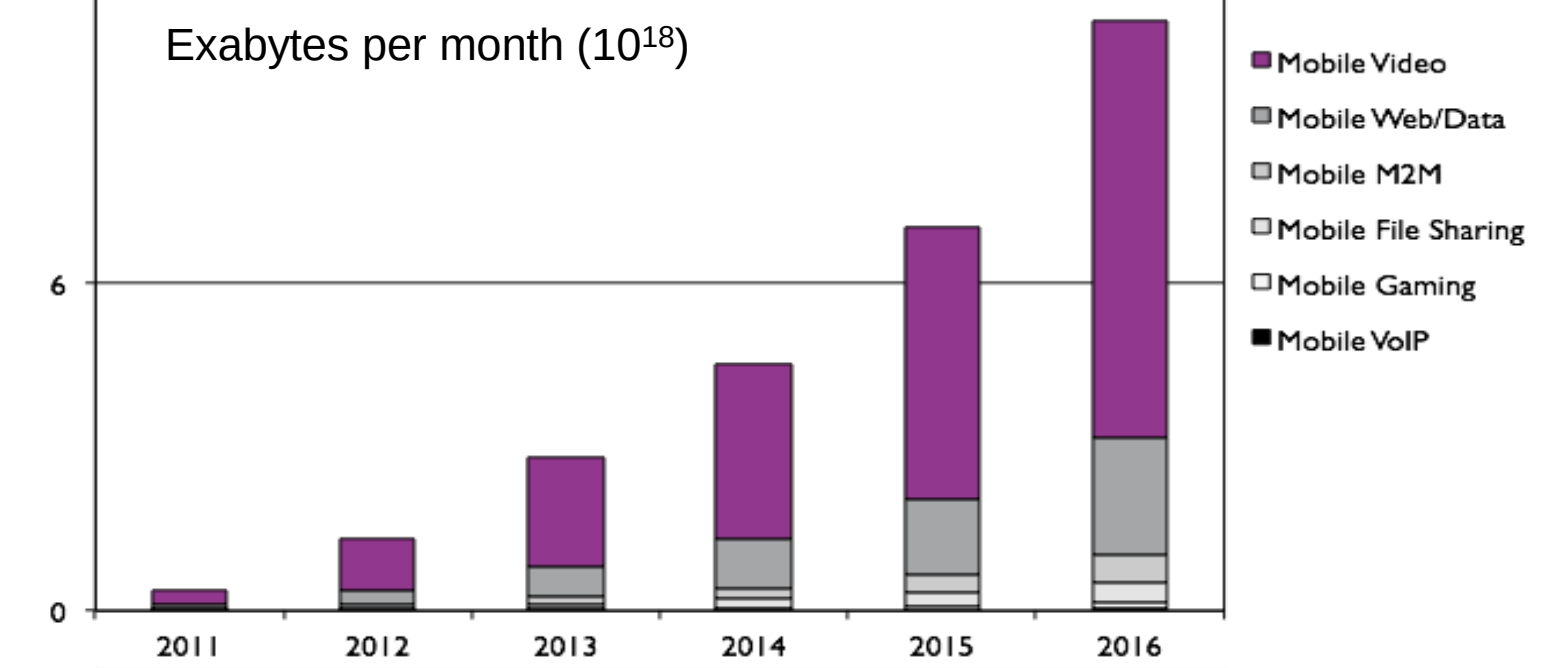


COST SCALING

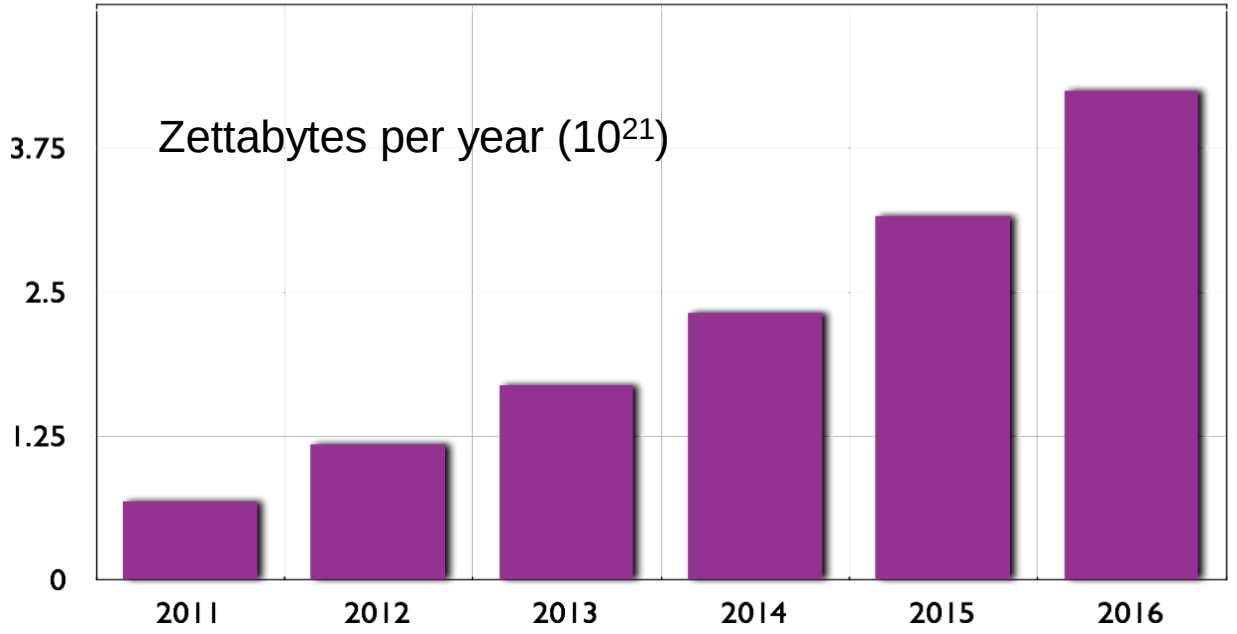
IMPROVED PERFORMANCE

GLOBAL TRAFFIC FORECAST

MOBILE DATA

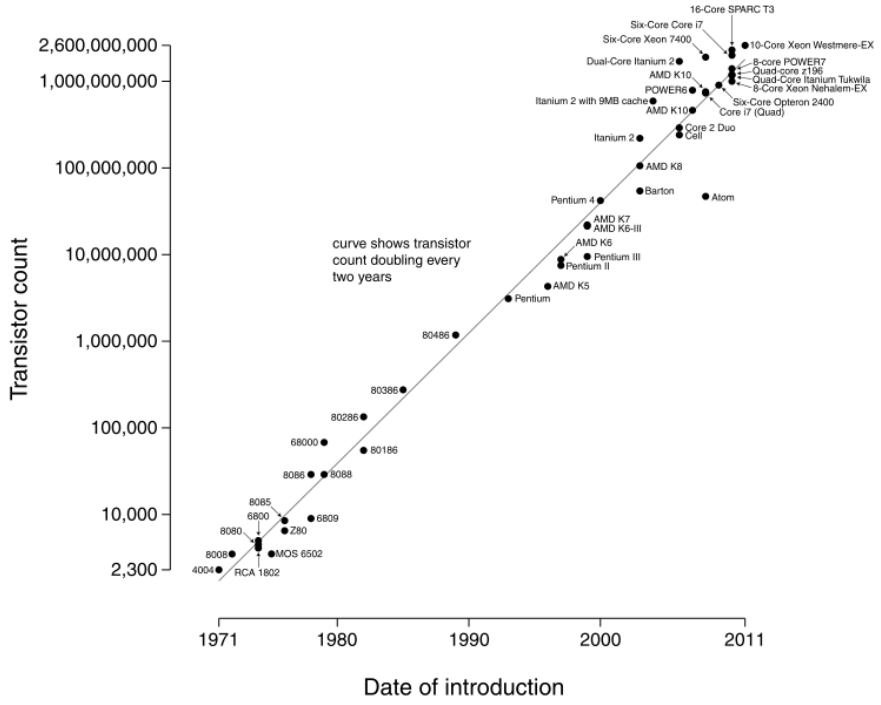


Cloud Traffic



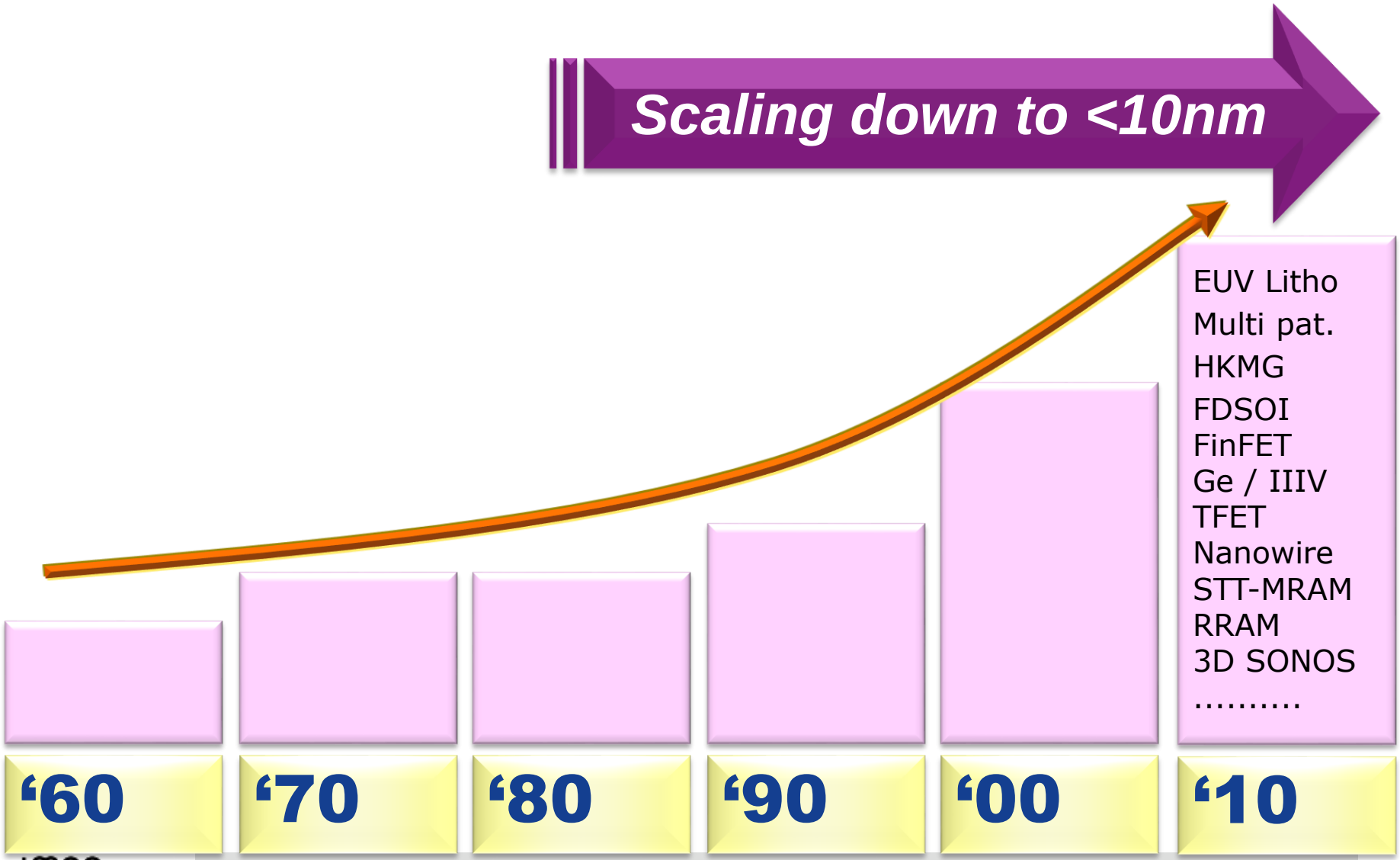
How will we make this happen at an affordable cost?

MOORE'S LAW CONTINOUS

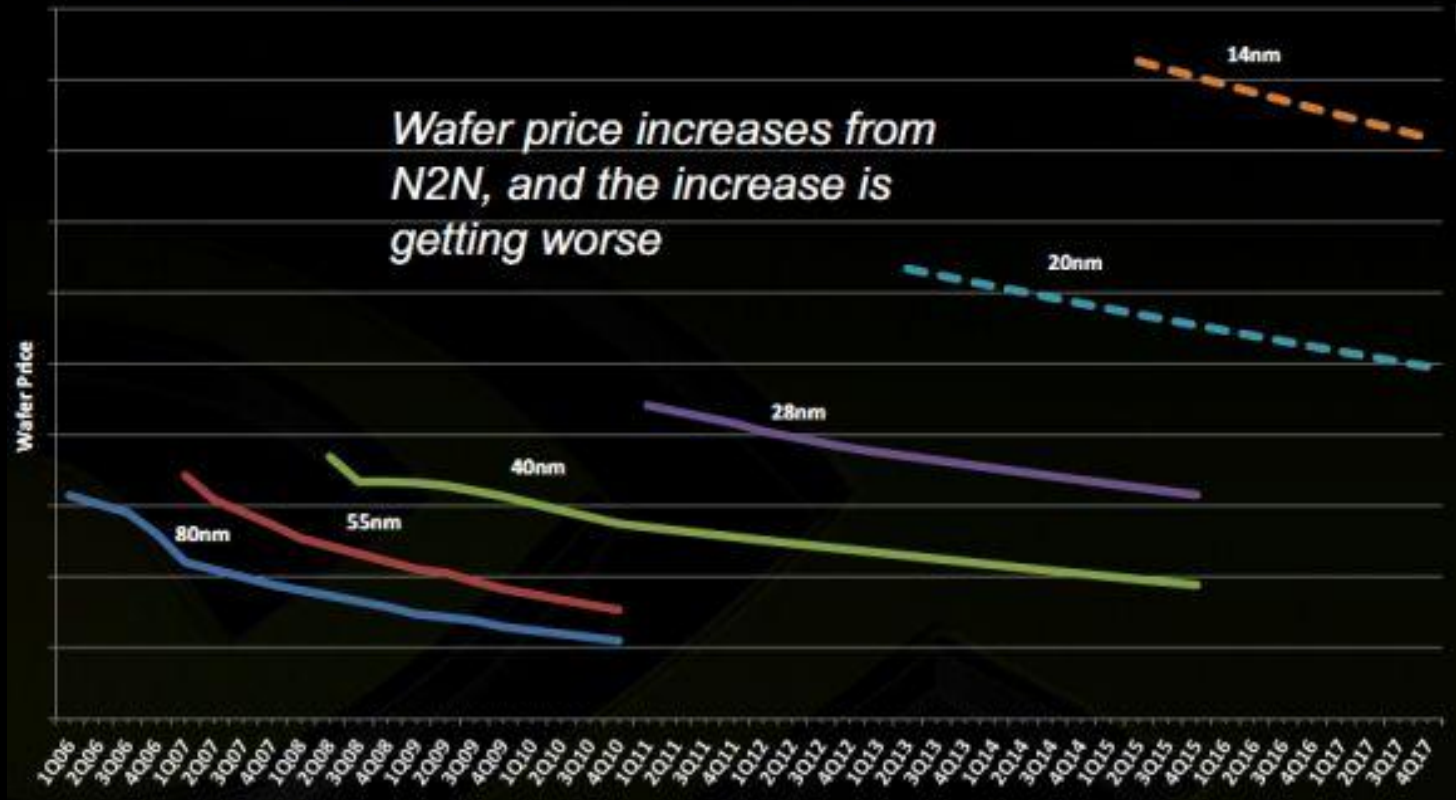


- 1970: Lithography enabled scaling
- 2002: Materials enabled scaling
- 14nm: 3D enabled scaling
- Wafer size scaling : 450 mm

INCREASING TECHNOLOGY COMPLEXITY



Wafer price is hiking up



- *The wafer price increase washes away the scaling benefit -> little saving in X'tor cost…need to lower CoO, simplify process, better yield...etc.. to incentivize Fab customers to 20 and 14nm.*
- *Collaborate to move to bigger (450mm) wafers*

Scaling & Scaling Challenges

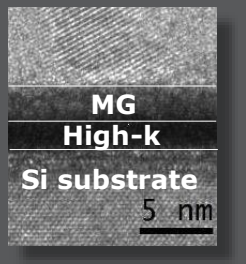
Imec Technology Roadmap

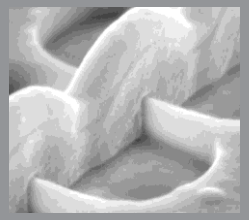
Wafer size scaling : 450 mm

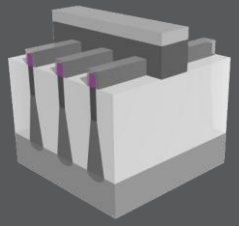
LOGIC SCALING ROADMAP

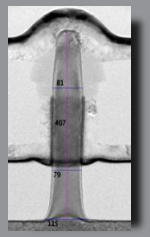
V_{dd}

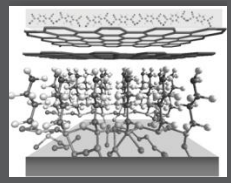
1.0-1.1V 0.9-1.0V	0.8-0.9V 0.7-0.8V	0.6-0.7V	0.5-0.6V	< 0.5V
MATERIAL	DEVICE	**MATERIAL**	DEVICE	**MATERIAL**
METAL GATE HIGH K	FINFET	HIGH MOBILITY CHANNELS	NANOWIRE/ TUNNEL FETs	2D MATERIALS





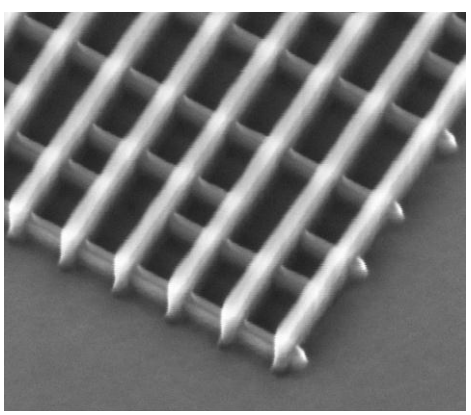


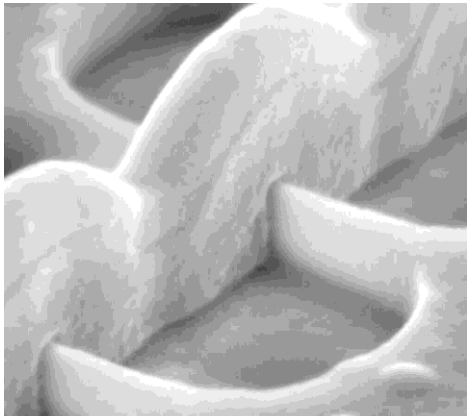


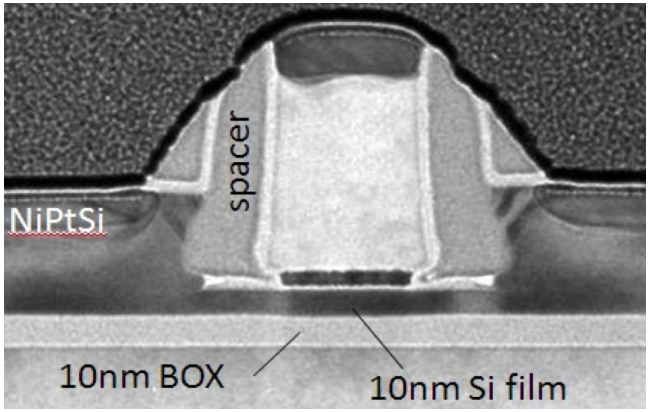


45nm — 32/28nm — 22/20nm — 14nm — 10nm — 7nm — 5nm — ... → Tech Node

LOGIC : 14 nm – 10 nm



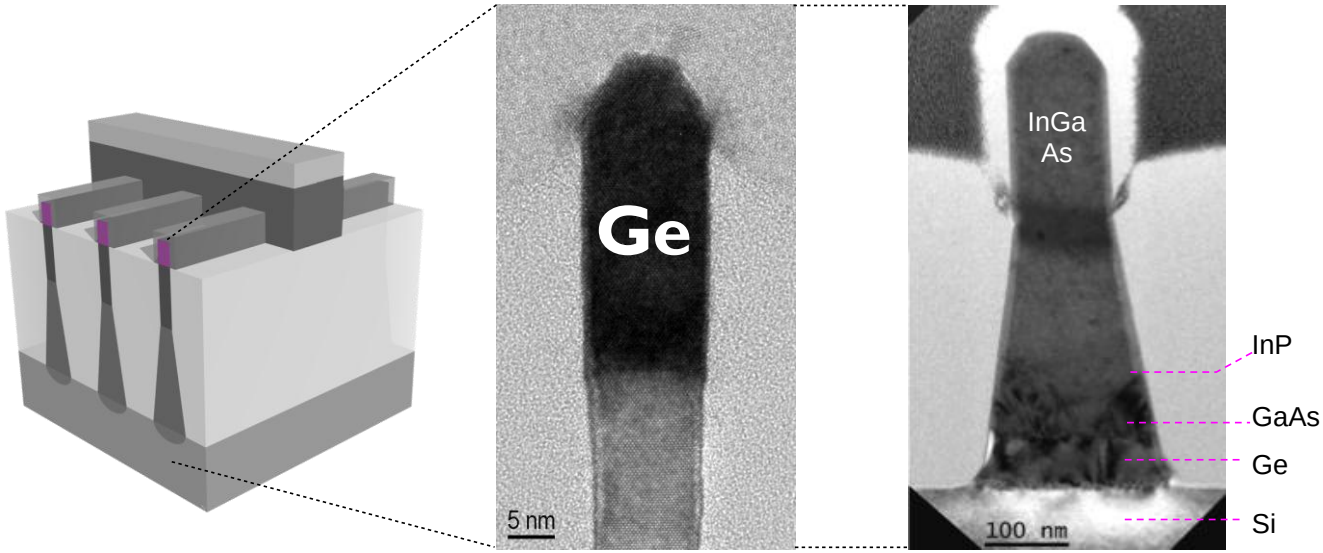




FinFET

- Conducting channel is wrapped by a thin silicon fin
- Fully depleted device: better short channel control
- Strain engineering to boost performance and scale down to 10nm

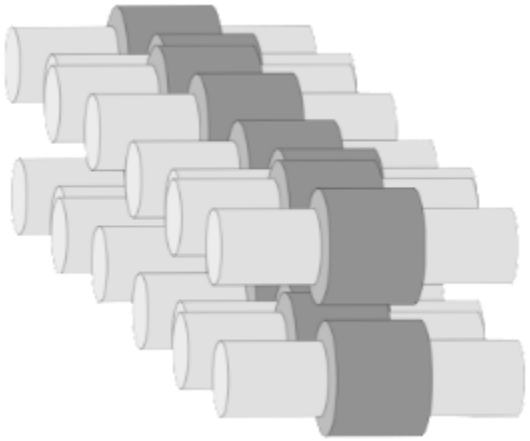
LOGIC : 10 nm – 7 nm



High-mobility channels

- Boost channel mobility by using Ge and III-V materials in the channel
- Two options: Ge-Ge and Ge-InGaAs for p-n channels

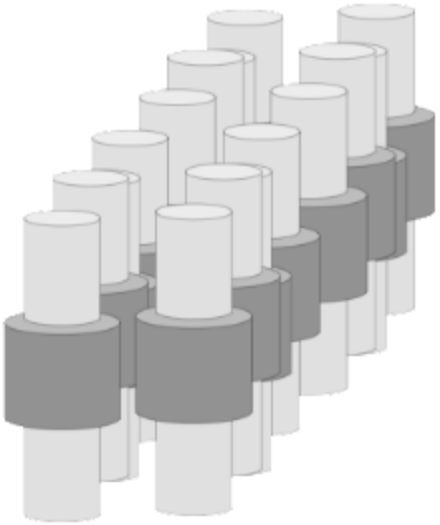
LOGIC : 10 nm – 7 nm

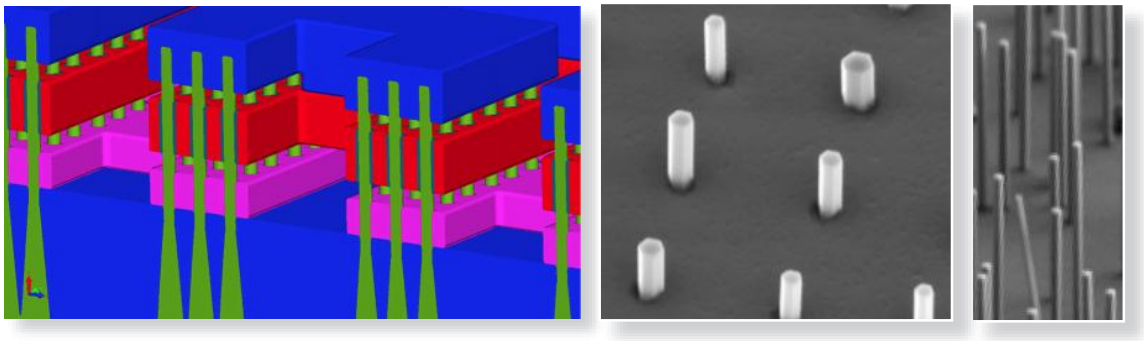


Gate-all around finFET

- Nanowire transistors with channel completely wrapped by the gate
- Superior gate leakage control

LOGIC : BEYOND 7 nm



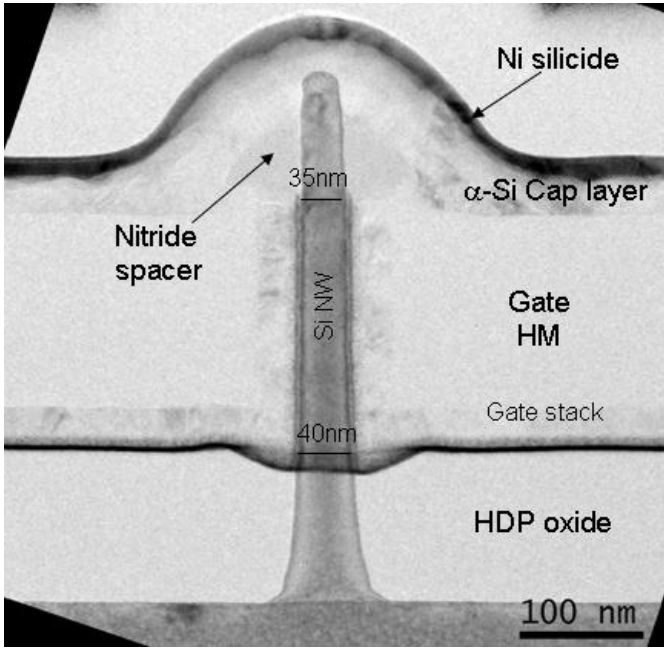


InAs Nano
wire
on <111> Si

Vertical finFET

- FinFET with vertical nanowires

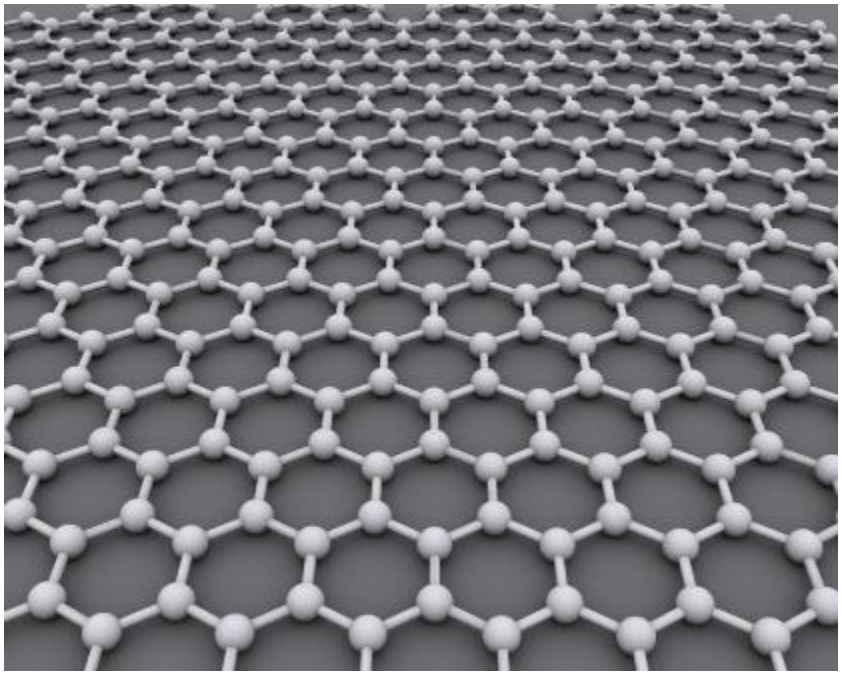
LOGIC : BEYOND 7 nm



TunnelFET

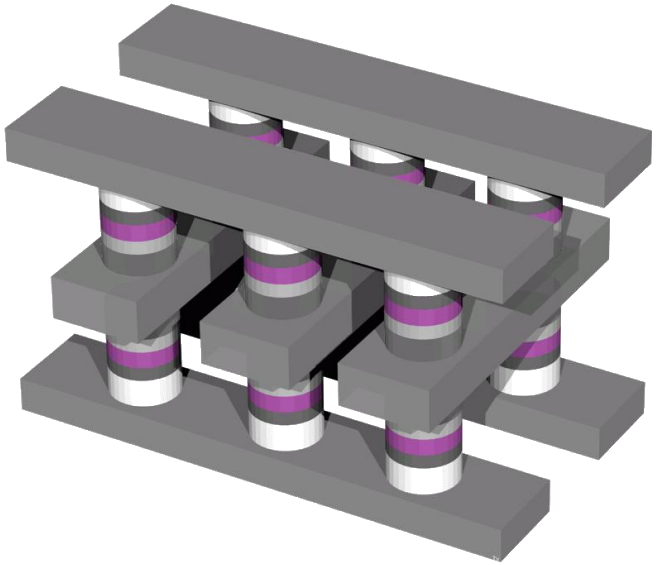
- Sub-60mV/decade subtreshold slope, allowing further reduction of supply voltage and power reduction

LOGIC : BEYOND 5 nm



- Many different options under research: Graphene FET, spintronics, BISFET, Ge tunnelFET, InAs tunnelFET, Graphene FET, spintorque, ...

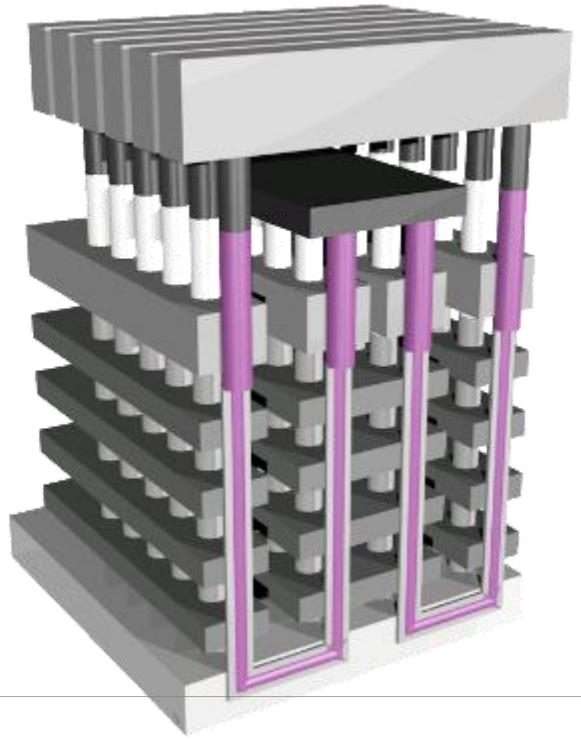
MEMORY : BEYOND 20 nm



STT RAM

- DRAM replacement beyond 20nm
- Non-volatile memory for both embedded and stand-alone applications
- Information is stored by using spin current of electrons instead of charge current

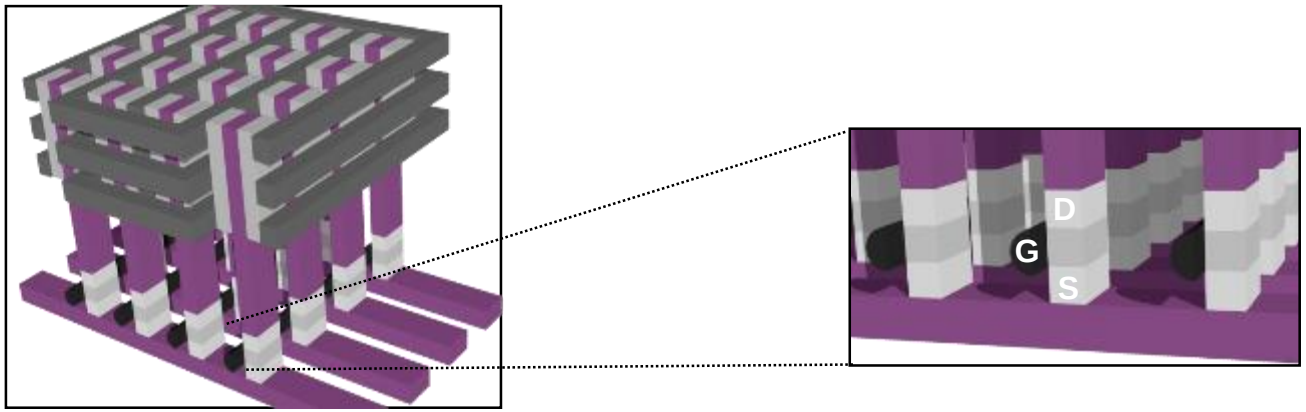
MEMORY :TO 10 nm



3D SONOS

- Flash replacement to 10nm
- Non-volatile memory
- Memory cells implemented in vertical plugs consisting of 8,16,32 ... stacks
- Successful processing of ‘macaroni cell’

MEMORY : BEYOND 10 nm

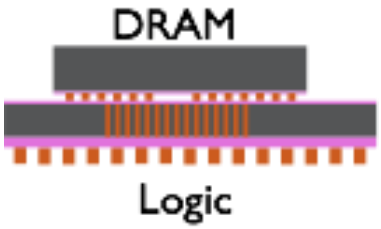


Resistive RAM

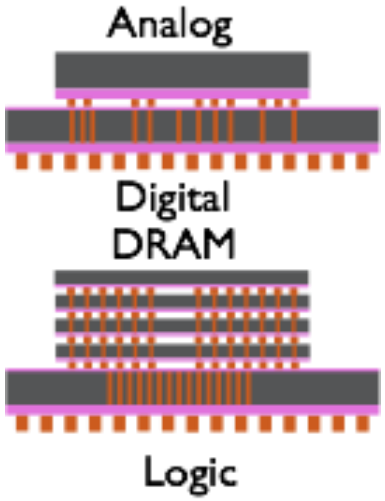
- Flash replacement beyond 10nm
- Non-volatile memory
- High speed, low energy, superior scalability, CMOS compatible
- Hourglass model:
  - Fundamental understanding of filament properties
  - Captures all main features of HfO2 RRAM device operation and reliability
  - Key for development of RRAM

3D enabled SCALING

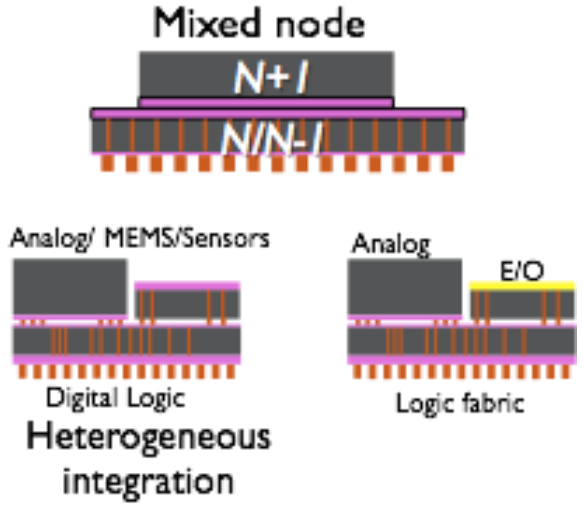
Gen.1
2012 - 2013



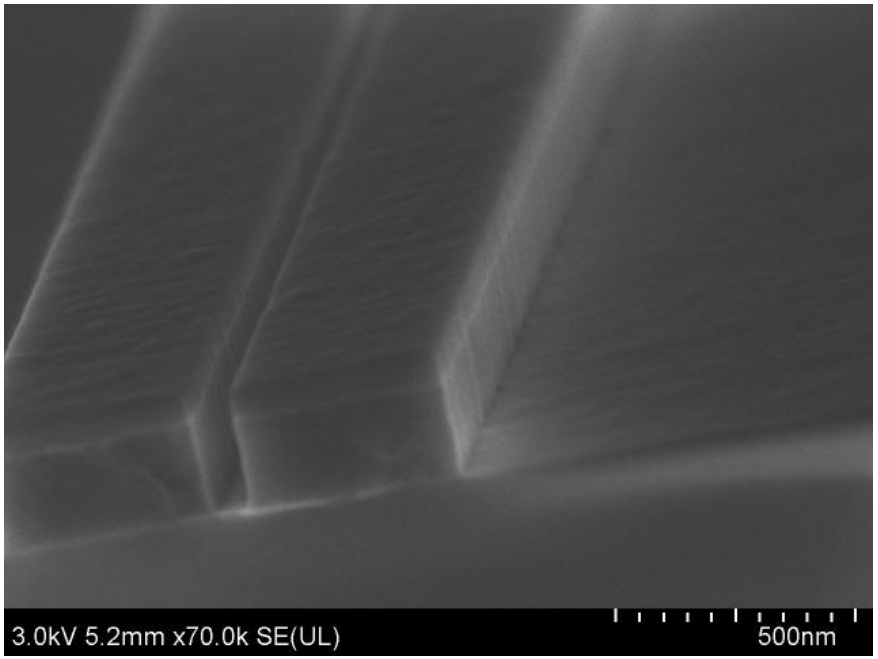
Gen.2
2014 - 2015



Gen.3
2016 - ...

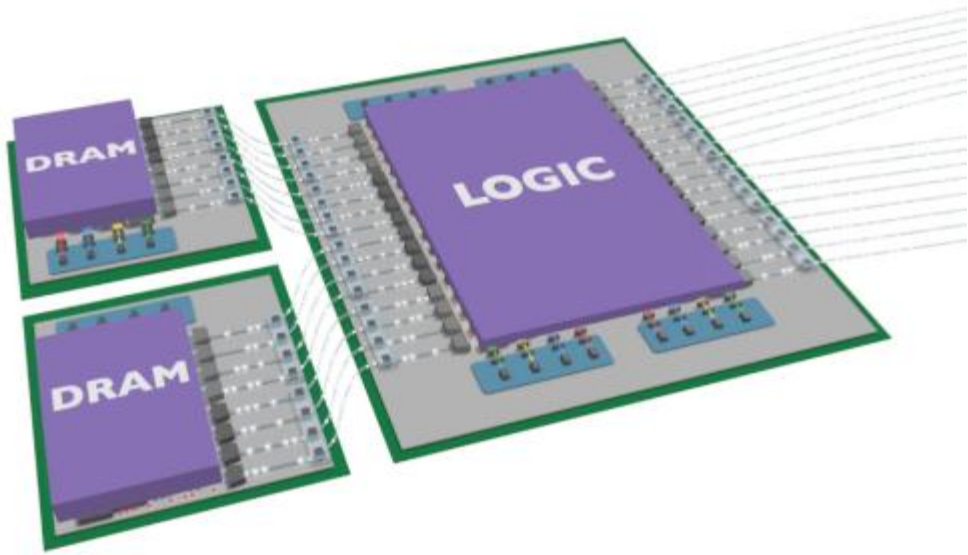


SILICON PHOTONICS



- World-first sub-100nm photonics components on 300mm Si technology with optical lithography in 28nm
- imec silicon photonics platform: cost-effective R&D of silicon photonics ICs for telecom, datacom, and life science applications

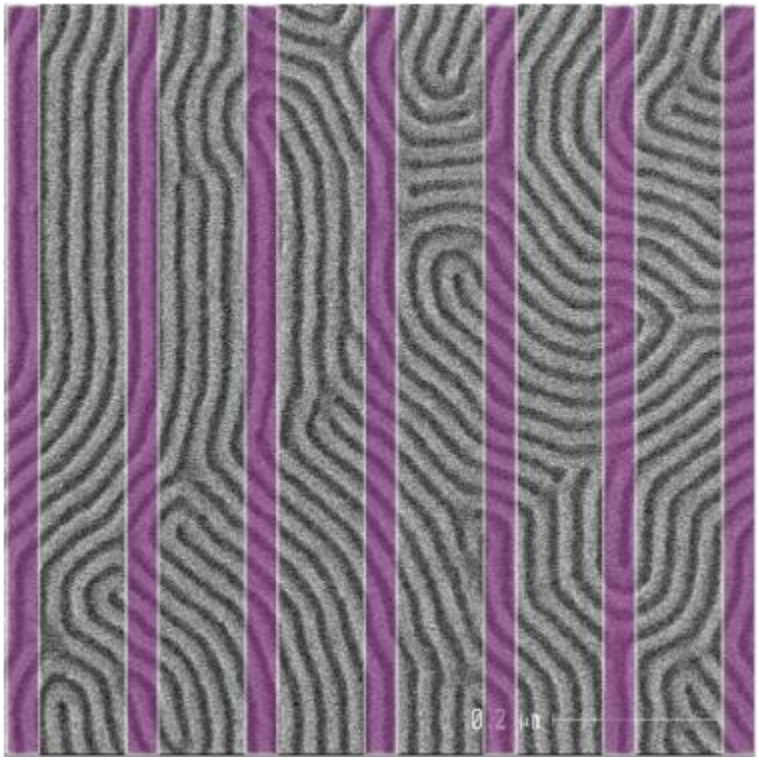
3D & OPTICAL IO



- Optical IO: extension of 3D stacking
- Further performance boosting, extreme high-bandwidth
- Optical interconnects using silicon photonics instead of electrical interconnects
- Fabrication of optical components by using CMOS processing techniques and equipment
- Need for best-in-class optical components

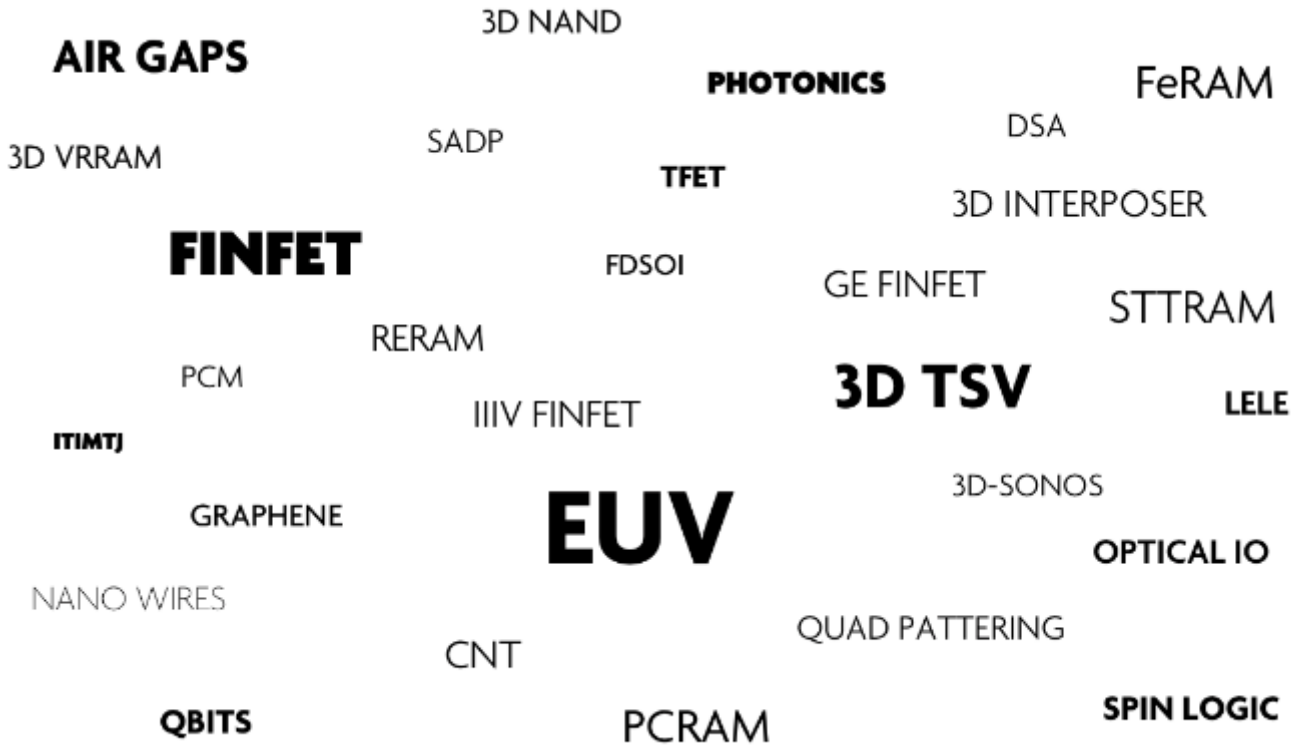
LITHOGRAPHY ENABLED SCALING
EUV : 13.5 nm LITHOGRAPHY

DIRECTED SELF-ASSEMBLY



- Extending optical lithography beyond current limits
- Promising candidate for more effective frequency multiplication by using block co-polymer chemistry
- True bottom up approach for high resolution patterning

RESEARCH COMPLEXITY

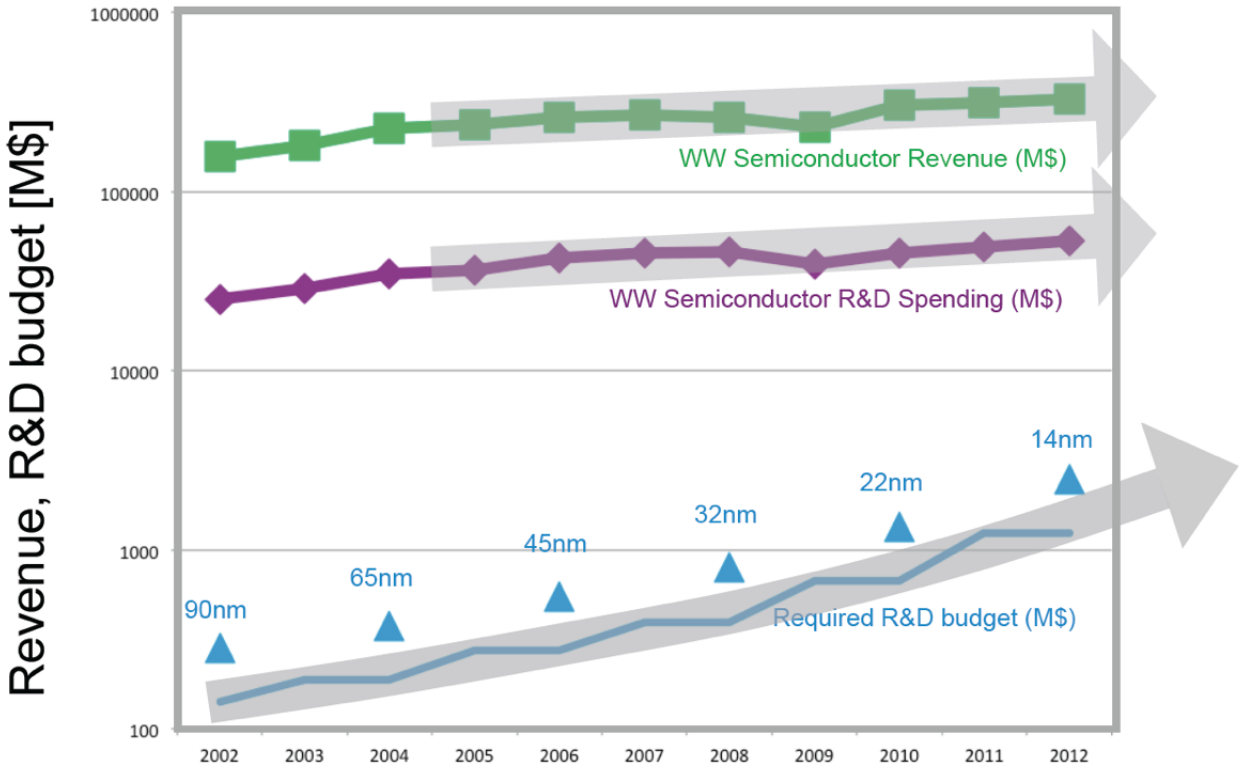


Technology complexity increases:

- Multitude of material options & processing techniques
- Combination of new materials & architectures
- System/circuit level implications

Increasing amount of options

INCREASING R&D COST



source: IHS iSupply
Sematech Report
IBS 2011

CORE CMOS PARTNERS

Logic & Memory IDM & Foundries

intel · SAMSUNG · tsmc · TOSHIBA SanDisk · Micron · SK hynix · GLOBALFOUNDRIES

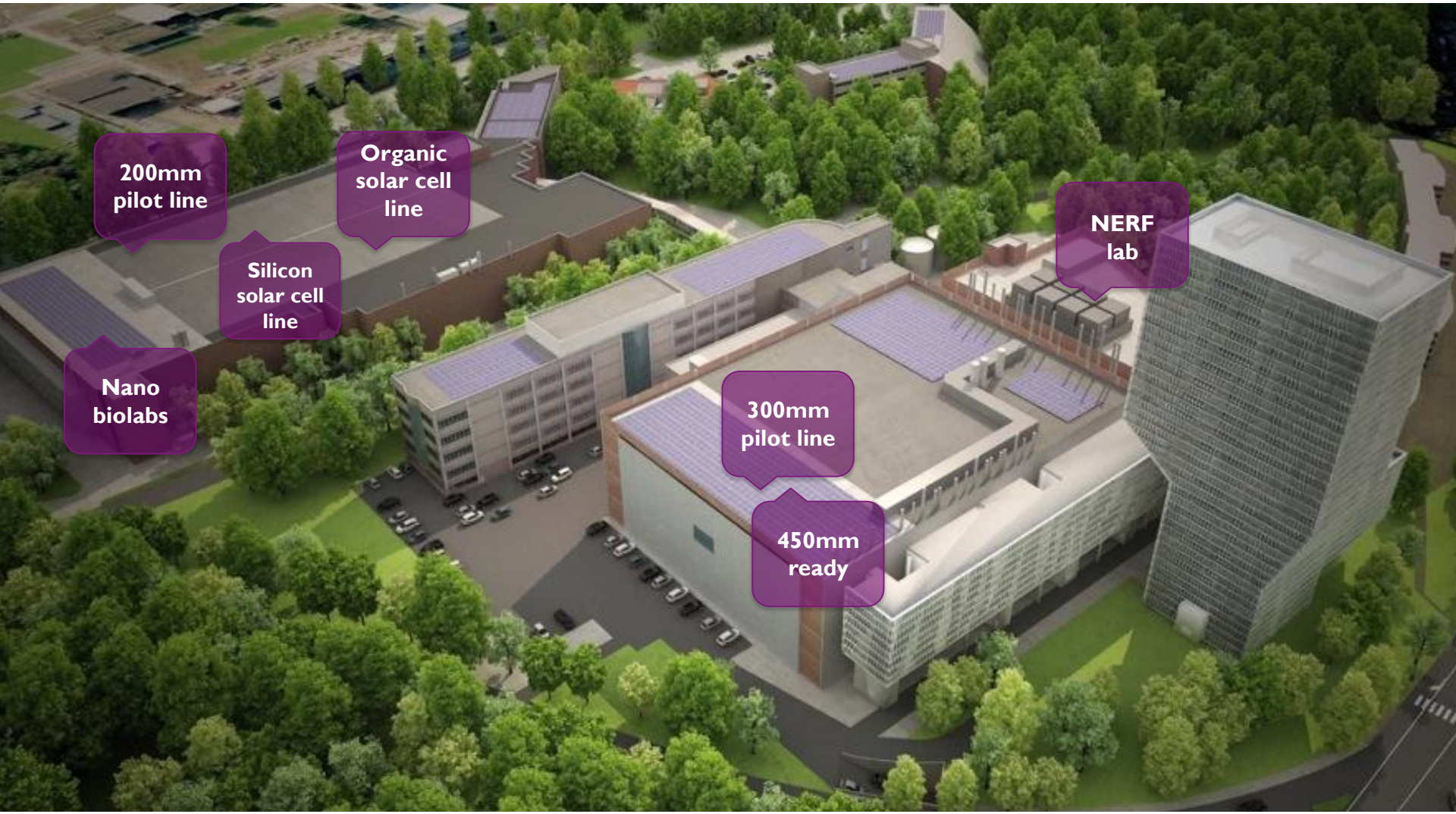
Fablite & Fabless & OSAT

Panasonic · QUALCOMM · SONY · Amkor Technology · NVIDIA · UTAC · FUJITSU · XILINX · ALTERA

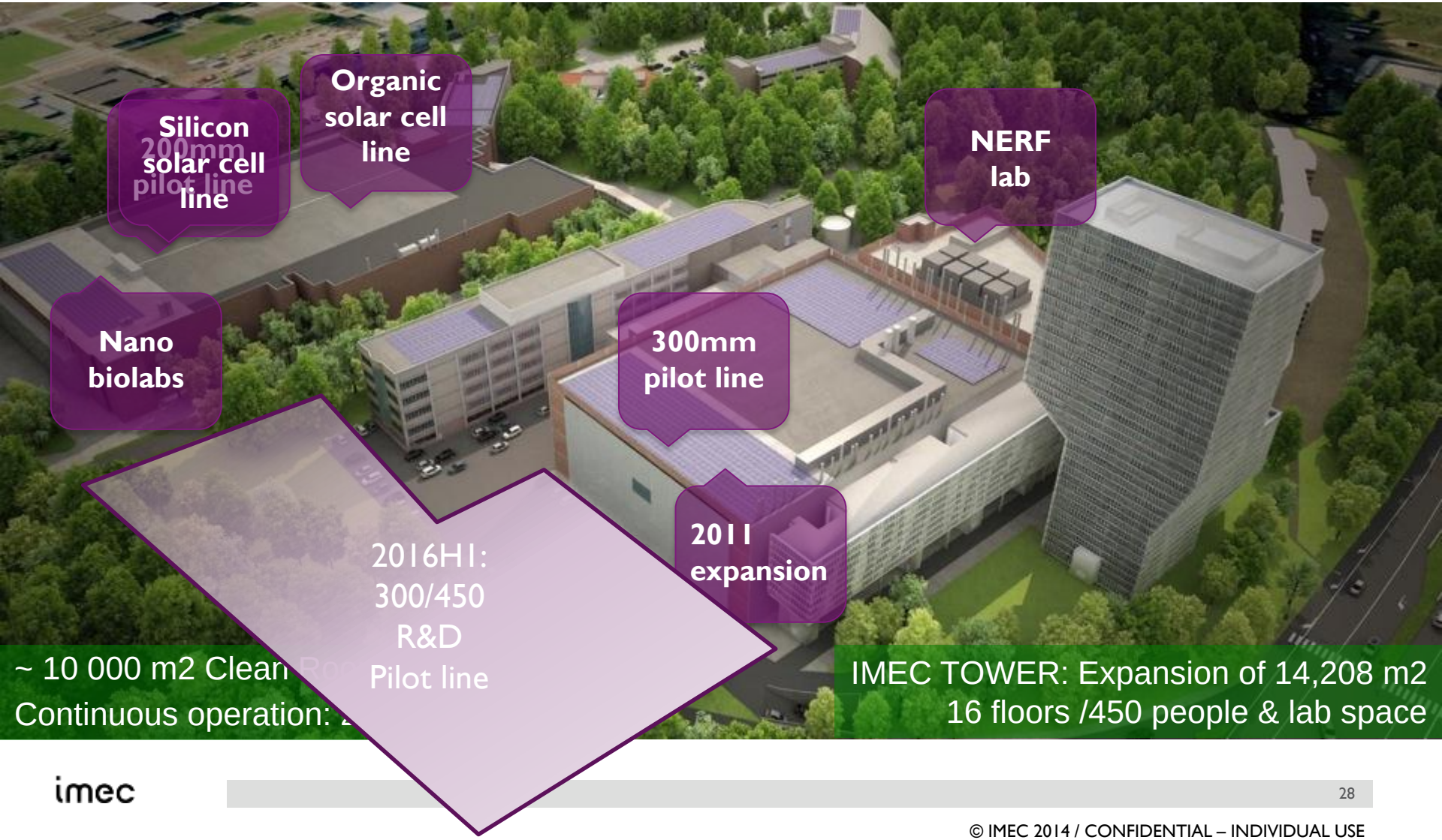
ASML · ASM · APPLIED MATERIALS · Lam RESEARCH · KLA-Tencor · TEL · SOKUDO · SUSS MicroTec · SCREEN · Mentor Graphics · brewer science · JSR · TOPPAN · NuFlare · SEMILAB · OXFORD INSTRUMENTS · RIXTRON · Ultratech · cadence · FUJIFILM · siltronic · SunEdison · umicore · DNP · NISSAN Chemical · FEI · DOW CORNING · ZEISS · RIBER · HITACHI · SYNOPSYS · AZ Electronic Materials · tok · Soitec · AGC · DUPONT · DISCO · Hitachi Chemical · BASF · CASCADE · Entegris · nanometrics · Sumitomo · DONGJIN · EBARA · ATMI · Voltaix · Canon · CANON ANELVA · JX Nippon Mining & Metals · PVA TePla · DOW · ThinMaterials · Quantum Wise · EDWARDS · JORDAN VALLEY · Henkel · BRUKER · Camtek · ziptronix · CAPRES A/S COPENHAGEN APPLIED RESEARCH

Share the R&D effort = Cost Sharing

STATE-OF-THE-ART RESEARCH FACILITIES



EXPANSION OF OUR RESEARCH FACILITIES



CONSTRUCTION START H1 2014
CONSTRUCTION FINISH END 2015

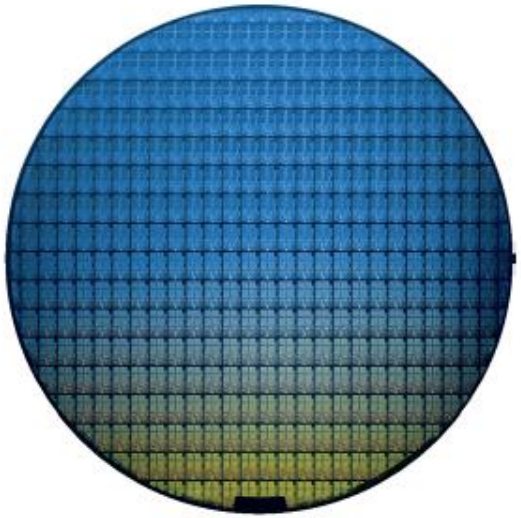
imec

EEM450PR

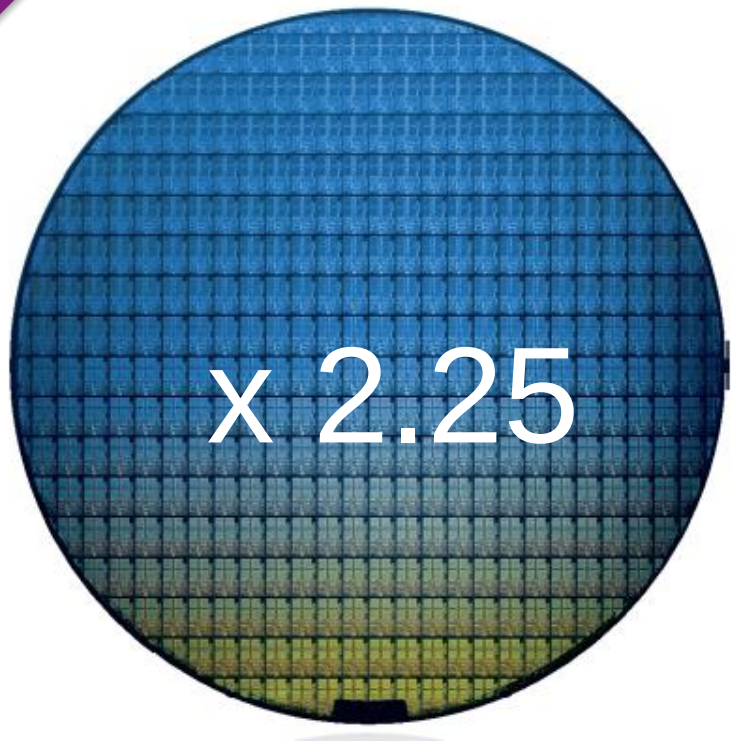
Scaling & Scaling Challenges

Imec Technology Roadmap

Wafer size scaling : 450 mm



300 mm



450 mm

Does Wafer Size Migration result in cost scaling?

WAFER BASED PROCESSING

DEPOSITION,
ETCHING,
CLEANING, ...

EFFICIENCY BENEFIT: 2.25x

BODY
WAFER HANDLING
PROCESS OPTIMIZATION

(SERIAL) DIE BASED PROCESSING

LITHOGRAPHY,
IMPLANT,
INSPECTION, ...

EFFICIENCY BENEFIT: 1x
(2.25x reduced wph)

BODY
WAFER HANDLING
PROCESS OPTIMIZATION
THROUGHPUT

Scaling yields increase of die based processing

IMEC WAFER SIZE CONVERSION HISTORY

1984: 4” Pilot-line

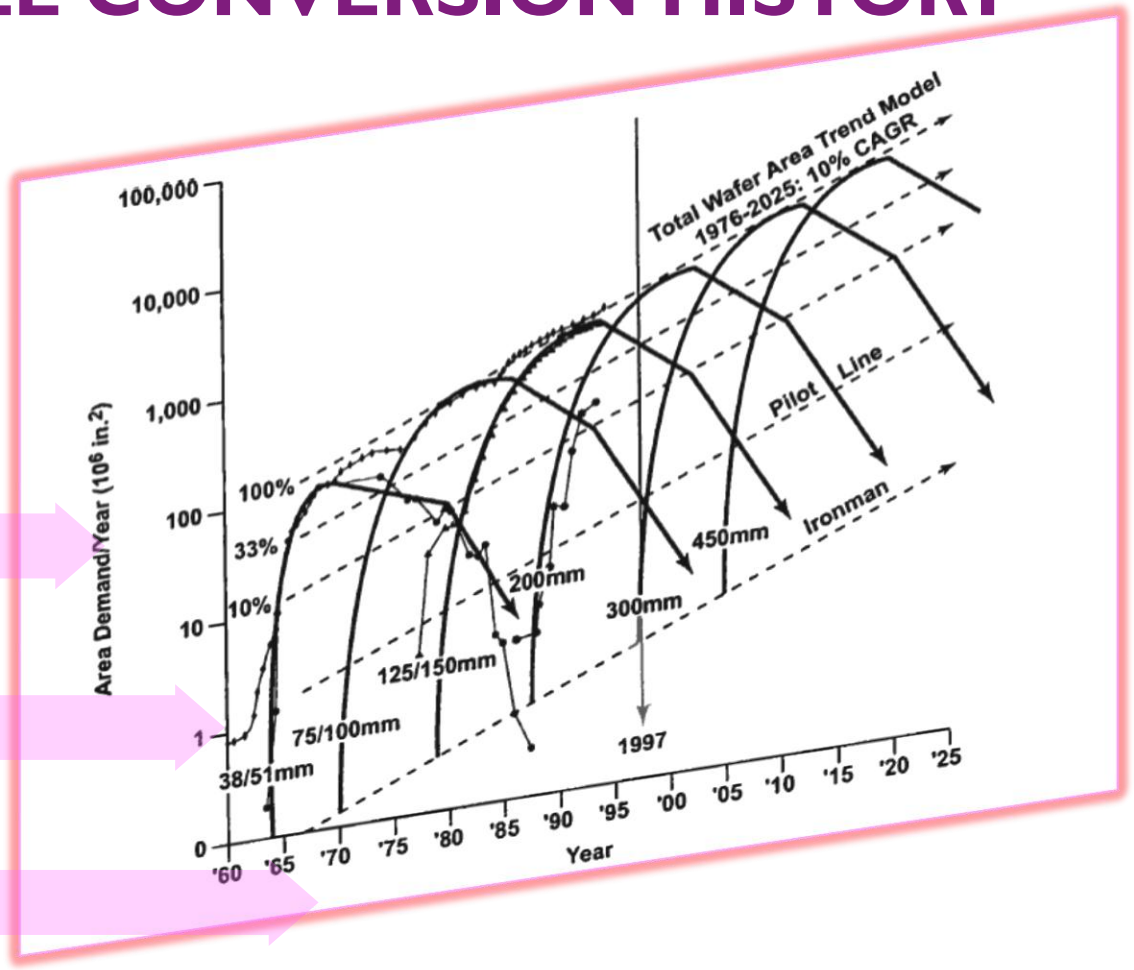
1986: 5” Pilot-line

1993: 6” Pilot-line

1999: 8” Pilot-line

2004: 12” Pilot-line

2016: 450 mm Pilot-line



Imec 450 mm migration

ENIAC
FP7
Flemish Gov't
Industry

KET
HORIZON 2020
ENIAC
Flemish Gov't
Industry

2013	2014	2015	2016	2017	2018	2019	2020

450mm Equipment roadmaps

450mm Pilot

450mm Production

phase 1

Selected Module assessment

300/450mm
imec Fab1

450 mm ready facility @ imec
EEMI450, SOI450, NGC450, EEM450PR, …

Phase 2

Process & Device development in Full flow facility

300/450mm
imec Fab2

gradually 300/450 mm PILOT R&D facility @ imec

WAFER SIZE SCALING : 450 mm

- 450 mm migration is feasible!
- Does 450 mm migration result in a significant cost saving?
- 450 mm migration waiting for industry commitment.

LET'S WORK TOGETHER

THANK YOU!